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Review of the Architectural Changes of Conventional MOSFET Structure to control Short Channel Effects

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Abstract

With the advancement of nanotechnology, conventional MOSFET structure is replaced by newer architectures like ON- insulator structures, asymmetric source/drain structures, use of III-V semiconductors, double gate (DG) and gate-all around (GAA) structures, FINFETs etc to control the short channel effects. Improvement of device performance is further looked upon by replacing conventional SiO2 with high-k dielectric materials like Al_2O_3, ZrO_2, HfO_2.This paper clearly reviews this architectural progress of MOSFETs necessary to project MOSFET as the suitable device for low power, high speed applications.

Keywords: ON-insulators; asymmetric source/drain; III-V semiconductors; DG and GAA, high-k dielectric

1. Introduction

Short-channel effects (SCEs) in MOSFET devices are the effects that occur when the device dimensions are scaled down to the range of nanometres [1]. Scaling improves threshold voltage and ON-current of the devices. However, lowering of threshold voltage increases the OFF-current, thereby increases SCEs. Various physics-based mathematical models and simulations are now conducted on the scaled devices to compare devices performances at advanced technology nodes. The results of the models and simulations create the pathway for the design of several CMOS circuits. [2]

Several architectural changes are now adopted to control this unwanted effect of leakage current. In 2025, Ahmed S. Al-Jawadi et.al [3] proposed a novel MOSFET design to overcome short channel effects in nanoscale devices. The design uses an asymmetric high-k gate dielectric (HfO_2), where the oxide thickness is different on the source and drain sides. The results show that the proposed structure improves performance by reducing leakage current by about 12%, increasing ON current by around 13%. The asymmetric structure also improves electric field distribution, giving better control over the channel and reducing short channel effects. The study successfully demonstrates that using an asymmetric gate dielectric structure in a 20 nm MOSFET significantly enhances device performance compared to conventional designs. These leads to higher ON current and lower leakage current, better ION/IOFF ratio, reduced DIBL and improved subthreshold swing. Thus, the proposed design effectively reduces short channel effects, and it is suitable for low-power, high-speed nanoscale

applications. Double-gate Silicon based n-FinFETs are an area of new-age study. FinFETs give better control over the channel and work better with modern technology but do suffer from Drain Induced Barrier Lowering and leakage. Use of III-V semiconductor materials instead of Si improves the performance of nanoscale devices. The goal is to make nanoscale FinFETs work better by using III-V semiconductor materials to reduce channel effects [4-5].
This architectural advancement is projected in this paper to project MOSFET as future device fat advanced technology nodes.

2. Review of Architectural Changes

A. Silicon-on-Insulator Structure (SOI)

In 2012, Priyadarshini Jena *et.al* [6] used the SILVACO ATLAS TCAD tool to design and study SOI-MOSFET devices at micrometer scale. The work emphasised on improving device performance by changing the thickness of silicon and oxide layers. These changes affect the threshold voltage and current–voltage behavior which in turn help in reducing common CMOS problems like parasitic capacitance and latch-up

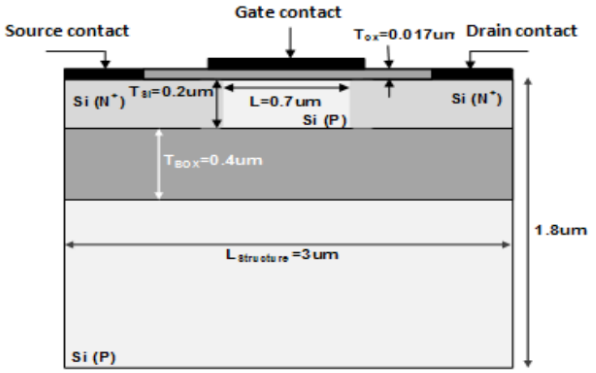


Figure 1: Cross-sectional figure of SOI-MOSFET [6]

In 2015 Shakti Verma, *et.al* [7] explained the main physical limitations of traditional bulk silicon MOSFETs, such as high power loss and lower carrier mobility. They studied Silicon on Insulator (SOI) technology as a better and high-performance option for future electronic devices. Their work described the basic features of SOI MOSFETs and highlighted their benefits, including better isolation, faster switching speed, and resistance to latch-up and radiation effects. These advantages come from the buried oxide (BOX) layer, which helps in reducing unwanted parasitic capacitance. They concluded that SOI technology is more suitable than bulk silicon for nanometer-scale devices and low-voltage operations. However, they also pointed out that more accuracy and improvements are needed to reduce issues like kink effect, self-heating, and short-channel effects, so that better frequency performance and lower power consumption can be achieved.

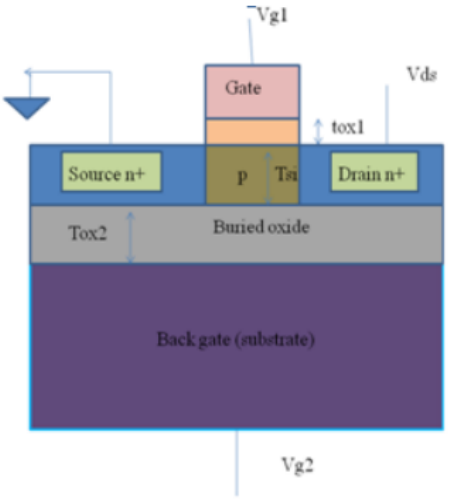


Figure 2: Structure of an SOI n-MOSFET [7]

B. III-V-On-Insulator Structure (XOI)

In 2016, Jianqiang Lin *et.al* [8] studied on body self-aligned InGaAs MOSFETs. These devices were built on a structure called III-V-On-Insulator with a silicon active substrate, also known as III-V-OIAS. This structure helps in adjusting the threshold voltage of the device. When the device is turned off, applying a positive voltage between the body and source reduces drain-induced barrier lowering, but it also increases the subthreshold swing. On the other hand, when the device is turned on, this voltage improves the series resistance. The study also showed that electrons can move in two different ways due to scattering at the front and back sides of the channel. It concluded that III-V-OIAS technology is very useful for power and high-performance VLSI applications. They further explained that applying voltage between the body and source is beneficial. It can make the threshold voltage more positive and improve (sharpen) the subthreshold swing without increasing gate leakage, which is a major issue. This means III-V-OIAS technology can help reduce power consumption when devices are idle.

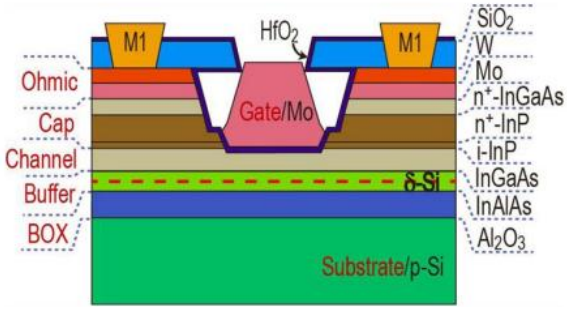


Figure 3: Cross-sectional schematic of InGaAs MOSFET on III-V-O-I with active silicon substrate [8]

C. Double Gate Structure

In 2014, Neetu *et.al* [9] studied the simulation of a Double Gate (DG) MOSFET at the 32 nm technology node. The goal was to reduce performance problems caused by scaling, such as higher Drain Induced Barrier Lowering (DIBL), gate leakage, and subthreshold slope issues, which happen due to weaker gate control over the channel. To solve this, they used a DG structure that adds another gate below the channel to improve gate control (coupling). This approach helps to overcome the limits of traditional scaling methods like reducing oxide thickness or using high-K materials, which can increase power loss or cause compatibility issues. After measuring and analyzing different parameters like threshold voltage (V_T), drive current (I_{ON}), and transconductance, the simulation results showed that the device can effectively reduce short-channel effects. It achieved a threshold voltage of 0.27 V at a drain voltage of 1.2 V and showed a much better I_{ON}/I_{OFF} ratio.

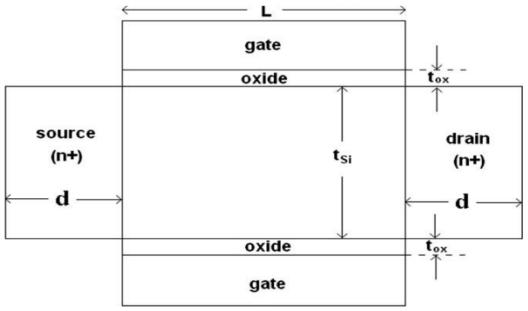


Figure 4: Structure of double gate MOSFET [9]

In 2014 A.Balhara et.al [10] worked on the design and simulation of a n-channel symmetric Double-Gate (DG) MOSFET with an 80 nm gate length. They used a high-k material (TiO_2) instead of the traditional SiO_2 to reduce leakage and short-channel effects like Drain Induced Barrier Lowering (DIBL) and channel modulation. The results of simulation showed higher drain current and lower subthreshold swing and leakage current which concluded that the double-gate structure gives better electrostatic control.In conclusion, their study found that even though scaling lowers the threshold voltage, the high-k DG-MOSFET is still a strong and reliable option for low-power and high-performance nanoscale devices. However, proper device design and optimization are needed to keep the parameters within acceptable limits.

In 2026, Pallabi Pahari et.al [11] presented a detailed TCAD simulation study to improve Double-Gate Tunnel Field-Effect Transistors (DG-TFETs) for ultra-low-power VLSI circuits and high-sensitivity uses like biosensing. They improved the device by carefully adjusting four main design factors: gate dielectric materials, silicon channel thickness, temperature, and channel materials. The study showed that DG-TFETs can go beyond the 60 mV/dec limit of traditional MOSFETs by using band-to-band tunneling (BTBT). The results showed that using high-k materials like HfO_2 and proper scaling of the device body helps to achieve a very low subthreshold swing of 31.4 mV/dec, a threshold voltage of about 0.46 V, and a very high I_{ON}/I_{OFF} ratio (from 2.2×10^{11} to 4.5×10^{11}). This leads to fast switching and very low leakage current. Finally, the study concluded that DG-TFETs are thermally stable, scalable, and a better alternative to traditional MOSFETs for future semiconductor technologies.

D. Gate All Around Structure (GAA)

Prateek and Samsher Singh in 2021 [12] focused on the Cylindrical GAA where the gate is wrapped around the channel. This gives the device good control over the electricity. They used a tool called the Silvaco Atlas device simulator, to look at a device that has a channel length of 50 nm and a channel thickness of 10 nm. It was found that the Cylindrical GAA setup is really good at reducing short-channel effects. It also makes the subthreshold swing better than the MOSFET designs. The results show that the Cylindrical GAA architecture is really good at controlling the electricity.

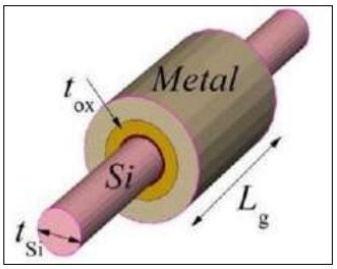
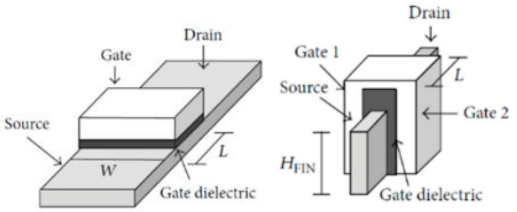


Figure 5: Schematic Structure of Cylindrical Gate All Around (GAA) MOSFET [12]

Lecheng Pan in 2024 [13] showed that the Gate-All-Around architecture is unique because it surrounds the channel on all four sides. For this design, 30% less power and 50% more drive current than FinFETs can be obtained. However, there are still some challenges to overcome. Managing short-channel effects and ensuring long-term reliability at the 2nm scale are hurdles. It was concluded that while Gate-All-Around FETs are poised to extend Moore's Law future advancements will require innovations in high-mobility channel materials, like Germanium and advanced 3D integration processes to realize the potential of Gate-All-Around FETs.

E. FinFET, TFET

In 2024, Koosha Karimi *et.al* [14] gave a detailed review of FinFET technology and showed that these 3D MOSFETs are better than traditional planar MOS devices. This is because they provide improved electrostatic control, better scalability, and lower power consumption By looking at past developments and different structural types—especially the shift from flat (horizontal) channels to vertical "fin" structures—the study explains how FinFETs reduce short-channel effects and leakage current problems. It also mentioned some manufacturing challenges, such as corner effects, parasitic issues, and difficulties in integration. It discusses new solutions like ground plane, bottom spacer, and negative capacitance FinFET designs to overcome these problems.

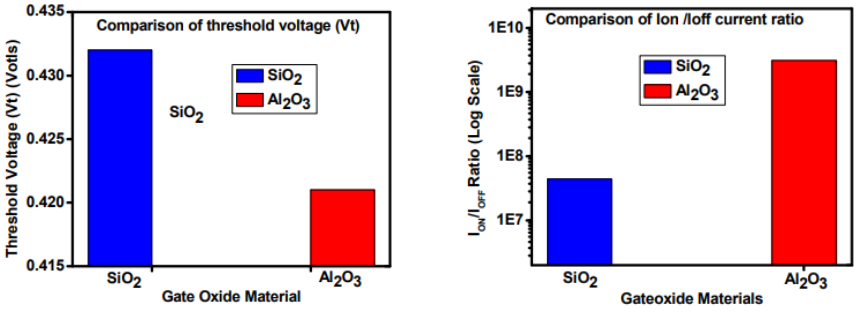


(a) (b)

Figure 6: Structure Schematic of (a) planar MOSFET and (b) FinFET [14]

In conclusion, the study highlights that FinFETs are very flexible and useful for new sensing applications. Their 3D structure helps in high-sensitivity detection in biological, chemical, and physical systems, as seen in advanced designs like ion-sensitive floating gate FinFETs.

In 2021, Rao Muhammad Asi *et.al* [15] studied the advancement of FinFET technology, which has emerged as a superior alternative to MOSFET due to its minimized short channel effects and enhanced performance in high-frequency applications. It presents a FinFET structure with analytical models for drain current, channel charge, and velocity, utilizing various dielectric materials with different underlap lengths for gate oxide. The performance of the oxide materials, specifically SiO_2 and Al_2O_3, is compared and concluded that Al_2O_3 offers lower threshold voltage and higher I_{ON}/I_{OFF} ratio, effectively reducing short channel effects. The study evaluates critical parameters and demonstrates the proposed models through the transfer and output characteristics of FinFET.



(a) (b)

Figure 7: Comparison of (a) Threshold Voltage (Vth) and (b) ION/IOFF, with (SiO_2, and Al_2O_3) [15]

In 2025, Shupeng Chen et.al [16] proposed a detailed review of Tunnel Field-Effect Transistors (TFETs) as a solution to the physical limits of Moore's Law and the increasing static power consumption in traditional MOSFETs, which are limited by a 60 mV/decade subthreshold swing. TFETs use the band-to-band tunnelling (BTBT) mechanism, which allows much sharper switching behavior. Because of this, they are very suitable for ultra-low-power electronics, biosensors, and optoelectronic applications. The study includes both experimental and simulation-based developments using different materials such as silicon (Si), germanium (Ge), III-V compounds, and 2D materials. It explains that Si and Ge have limitations due to wide bandgaps and high carrier mass, while 2D materials and heterojunction designs provide better electrostatic control and higher I_{ON}/I_{OFF} ratios. The report also discusses new device designs like dopingless (DL), junctionless (JL), and quasi-broken gap (QB-TFET), which help simplify fabrication and improve tunnelling performance. Finally, the study points out that although TFETs have strong potential for use with CMOS technology and non-volatile memory, there are still challenges to solve. These include process variations, interface trap issues, and gate leakage, which must be reduced for wider practical use.

F. Asymmetric source/drain Structure

In 2007, Jong Pil Kim *et.al* [17] demonstrated a new asymmetric MOSFET without light doping, which has been simulated by using the SILVACO simulator. A new asymmetric MOSFET utilizing to address the issues of the typical asymmetric process. A sidewall spacer gate and a table structure offers a self-alignment procedure,

effective scaling, and consistent performance. The simulated properties of the symmetrical and asymmetric MOSFETs have been matched. Essentially both asymmetric and symmetric MOSFETs feature an n-type channel and the same physical dimensions. Compared to the symmetric, better device performance is seen in the asymmetric MOSFET. This device configuration eliminates the Lightly Doped Drain(LDD) on source side, which has a significant impact on performance and scalability. The analysis focused on 50-nm asymmetric N-MOSFETs, revealing that the configuration without light doping (LDD) on the source side, utilizing a mesa structure, significantly improves driving current and device scaling. The self-aligned fabrication method ensures consistent channel lengths and performance of the asymmetric NMOSFET was compared to its symmetric counterpart, showcasing higher I_{ON} and reduced short-channel effects (SCE).

In 2022, Inyoung Lee *et.al* [18] examined the feedback field-effect transistor (FBFET), which utilizes positive feedback for enhanced switching properties, particularly a high on/off ratio and rapid state transition. In addition, the research suggests possible enhancements of the FBFET devices using asymmetric source/drain dopant concentration levels. Asymmetric FBFET demonstrates better electrical properties than symmetric one and, in particular, it is characterized by higher on/off ratio, while the threshold voltage (V_{TH}) and subthreshold swing (S) properties prove to be approximately equal under different channel length and thickness conditions, which means that an asymmetric FBFET is still effective when the FBFETs are scaled down.

Declaration of Conflicting Interests

The authors declare no potential conflicts of interest with respect to the research, authorship and publication of this article.

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