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Review of High-Performance Coding Schemes: Turbo, Polar, and Hybrid Codes for 5G and 6G

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Abstract

Error correction coding (ECC) is fundamental to achieving reliable communication over noisy channels. This review presents a unified analysis of Turbo codes, Polar codes, and their hybrid concatenated variants such as Turbo-Polar, LDPC-Polar, and Parity-Check-Concatenated (PCC) Polar codes, which are vital for 5G and beyond-5G (6G) systems. Turbo codes, introduced by Berrou et al., approach the Shannon limit through iterative decoding but suffer from latency and error floors. Polar codes, proposed by Arıkan, achieve channel capacity using polarization and are standardized in 5G New radio control channels, though their finite-length performance is limited. Recent studies, including concatenated Turbo-Polar codes, Polar Codes for future Wireless Communications, and Optimization of Iterative Decoding for Polar Product Codes, demonstrate that hybrid schemes combining iterative and belief-propagation decoding significantly improve Bit error rate performance with reduced complexity. Collectively, these advancements highlight the evolution of coding toward high-throughput, low-latency, and energy-efficient architectures, forming the foundation for next-generation communication networks.

Keywords: Turbo Codes; Polar Codes; Turbo Product Codes; Turbo-Polar Codes; LDPC-Polar Codes; Parity-Check-Concatenated Polar Codes; 5G New Radio;6G Communication Systems; FPGA Implementation.

1. Introduction

Error correction coding has become a cornerstone of modern digital communications, ensuring reliable data transfer over noisy channels. The evolution from Turbo codes, introduced by Berrou et al. in 1993, to Polar codes, proposed by Arıkan in 2009, and subsequently to hybrid concatenated schemes such as Turbo–Polar, LDPC–Polar, and Parity-Check-Concatenated Polar codes, reflects the continuous pursuit of capacity-approaching performance while maintaining manageable computational complexity. Turbo codes, as detailed in [1], have enabled data-rate evolution from megabits per second (Mb/s) to beyond 100 gigabits per second (Gb/s) and have been widely investigated in FPGA-based design studies. While they achieve near-Shannon-limit performance through iterative decoding, they suffer from error floors and increased latency at high data rates. Polar codes, as discussed in “A Golden Decade of Polar Codes” and related decoding

research, achieve capacity via channel polarization and are now standardized in 5G new radio control channels, though their performance declines at short block lengths. To address these limitations, hybrid schemes such as Turbo-LDPC-Polar and Polar codes—reported in "Concatenated Turbo-Polar Codes," "Optimization of Iterative Decoding for Polar Product Codes," and Polar Codes for Future Wireless Communications"—merge iterative and belief- propagation decoding principles to enhance BER/BLER performance, scalability, and throughput. Collectively, these developments form the foundation of 5G/6G communication systems, advancing toward highly reliable, low-latency, and energy-efficient networks [1].

2. Evolution of turbo codes and turbo decoder architectures

Turbo codes were introduced by Claude Berrou and colleagues as a practical application of parallel concatenated recursive systematic convolutional encoders separated by an interleave. The basic principle relies on exchanging extrinsic information between decoders in iterative loops, substantially improving convergence compared to serial concatenation. Initially adopted in 3G and 4G LTE, turbo codes have continued relevance in 5G and beyond, primarily due to their robustness, adaptability, and near-capacity performance across diverse channel models. According to Weithoffer et al. (2018), throughput requirements have escalated from 1 Mb/s in UMTS (1999) to >100 Gb/s in next-generation systems, driving new parallel and pipelined architectures to meet the demands of ultra-high-speed data links. The Parallel MAP (PMAP) and Fully Parallel MAP (FPMAP) architectures form the basis for modern turbo decoders. In PMAP, sub-blocks of codewords are decoded concurrently, while FPMAP extends this to the extreme processing one trellis step per clock cycle for maximum parallelism. However, excessive parallelism degrades error performance at high code rates and increases area complexity [1]. The pipelined XMAP and fully unrolled UXMAP architectures mitigate these limitations by functional parallelization. UXMAP pipelines entire iterations, enabling throughputs exceeding 100 Gb/s on 28 nm technology with high area efficiency (4.34 Gb/s/mm^2) [2]. Such architectures mark a paradigm shift toward fully pipelined iterative unrolling, uniting algorithmic and hardware co-design to sustain scalability in future 6G systems [1]. Turbo polar codes use iterative row/column decoding through either hard-input/hard-output (HIHO) or soft-input/soft-output (SISO) algorithms. The Chase-Pyndiah algorithm remains dominant due to its balance between near-optimal performance and manageable complexity. Variants such as Fast Chase and Reduced Candidate Set decoders exploit Gray-ordered test sequences and adaptive reliability metrics to cut computation without degrading BER. The Liang et al. (2025) study introduces a compact candidate code set architecture that shortens the search space while compensating for performance loss via novel extrinsic information computation. Implemented on FPGA, the design achieves 1.37 Gb/s throughput with reduced decoding delay and memory conflicts [2]. The interleave-like memory allocation avoids contention in high-parallel hardware, marking a significant advancement for low-power, high-efficiency Turbo polar code decoders [3].

3.Turbo-Polar Codes (TPC/Polar Hybrids)

Polar codes are the first provably capacity-achieving codes for binary-input symmetric channels; however, SC decoding suffers from degraded BER performance at short block lengths [3]. To enhance practical performance, Turbo-Polar Codes combine the iterative feedback structure of Turbo Codes with polar code components, achieving better convergence and robustness. Proposed Punctured Turbo-Polar Codes (PTPCs) to achieve flexible code rates and lengths without performance degradation. By puncturing parity bits

asymmetrically and inserting zeros at the decoder, they maintained decoding compatibility while enhancing throughput. Using the Soft Cancellation (SCAN) decoder a low-complexity SISO variant of Belief Propagation PTPCs achieve comparable BER to unpunctured codes under AWGN channels, with reduced complexity and latency [4].

3.1.1 Advantages and Performance

Maintains BER parity with unpunctured designs. Asymmetric puncturing prevents error propagation. SCAN decoding offers low complexity and suitability for parallel hardware. Supports flexible payload sizes and adaptive rates critical for adaptive 5G/6G systems. The PTPC framework bridges the gap between theoretical polar coding efficiency and practical turbo code flexibility, making it a promising candidate for high-rate, low-latency communication scenarios [4].

3.1.2 FPGA-Based Turbo Encoder and Decoder Implementation

A complete FPGA-based turbo encoder/decoder designed via MATLAB Simulink and VHDL synthesis [5]. Their work provides critical practical insights. The turbo encoder comprises two parallel RSC encoders with an interleaver, achieving a base rate of 1/3, extendable to 1/2 through puncturing. The decoder uses SOVA and MAP algorithms, iteratively exchanging extrinsic information to refine bit decisions. Log-MAP and Max-Log-MAP approximations were employed to simplify hardware implementation without substantial performance loss. Bit Error Rate (BER) performance was assessed under variable: Code lengths, Iteration counts, Code rates, Decoding algorithms. Results indicated that increasing iterations improves BER up to a threshold beyond which gains diminish. MAP decoding achieves superior accuracy but higher computational cost, while SOVA offers an attractive performance-complexity trade-off. Results indicated that increasing iterations improves BER up to a threshold beyond which gains diminish. MAP decoding achieves superior accuracy but higher computational cost, while SOVA offers an attractive performance-complexity trade-off. This practical realization confirms that turbo architectures can be efficiently deployed on reconfigurable hardware, bridging theory with system-level implementation. The design enables scalability for software-defined radios (SDR) and 5G baseband processors requiring programmable forward error correction (FEC) acceleration [5].

Table 1: Comparative Discussion [1] [3] [5] [11] [14]

Aspect	**Turbo Codes**	**Turbo Product Codes**	**Turbo-Polar Codes**	**FPGA Implementation**
Structure	Parallel concatenation of convolutional codes	2D product of block codes	Parallel concatenation of polar codes	Hardware realization of T
Decoding	Iterative MAP / SOVA	Chase-Pyndiah / Reduced Candidate Set	SCAN / BP / Iterative	Log-MAP, SOVA
Complexity	Moderate	High (iterative HDD/SISO)	Moderate-Low	Hardware-bounded
Throughput	Up to >100 Gb/s (UXMAP)	1–10 Gb/s (modern FPGA)	Scalable with puncturing	Tested to hardware limits
Key Feature	Near-Shannon performance	High coding gain & self-detection	Flexible rates, low complexity	Real-time validation

3. Fundamental Principle of Channel Polarization

Arıkan's original Bhattacharyya parameter-based method efficiently constructs polar codes for the Binary Erasure Channel (BEC), but for channels like BSC or AWGN, more sophisticated approaches are required. Tal and Vardy (2013) proposed channel degrading and upgrading approximations that "sandwich" the true bit-channel between two tractable approximations. Their construction algorithm computes upper and lower error-probability bounds for each subchannel with linear complexity in block length, enabling efficient and provably capacity-achieving code construction. The Successive Cancellation algorithm, introduced by Arıkan, decodes bits sequentially using likelihood ratios. However, SC decoding performs poorly for short and moderate block lengths, where early bit errors propagate and degrade performance. To overcome SC's limitations, Tal and Vardy (2015) introduced SCL decoding, which maintains LLL candidate paths during decoding, selecting the most likely one at the end. The list size (L) controls the trade-off between complexity and performance. With moderate LLL (e.g., 32), SCL approaches Maximum-Likelihood (ML) performance [6]. Equations When concatenated with a Cyclic Redundancy Check (CRC), the CRC-aided SCL (CA-SCL) decoder significantly outperforms LDPC and Turbo codes at short block lengths, eliminating the error floor common to those codes. SCS decoding explores candidate paths dynamically based on likelihood ranking, providing flexible complexity scaling. Later improvements, such as adaptive SCL (A-SCL), adjust list size depending on channel reliability, reducing average decoding latency [7]. Recent research focuses on low-latency implementations of list decoders.

Introduced Fast SCL decoders utilizing Minimum-Combination Sets (MCS) for high-rate nodes like Single Parity Check (SPC) and Sequence Rate-1 (SR1) structures [8]. Thes methods pre-compute candidate paths, enabling parallel decoding and reducing latency by up to 68% without performance degradation a critical improvement for URLLC (ultra-reliable low-latency communications) in 5G. Efficient estimation of bit-channel reliability remains central to polar code construction. Tal & Vardy's degrading/upgrading framework offers an analytical foundation for arbitrary DMCs, while Monte Carlo simulation and density evolution (DE) methods refine reliability metrics under AWGN conditions. Quantization schemes limit alphabet size while maintaining accuracy, achieving near-optimal rate selection with linear-time complexity. Cyclic redundancy check concatenation improves minimum distance and aids in error detection. Cyclic redundancy check bits interact with the list decoder, providing a simple yet powerful genie-aided selection mechanism. CA-SCL codes now represent the standardized design for 5G control channels (as per 3GPP New radio specifications) [9]. In practice, rate matching adapts the fixed-length polar codes to variable packet sizes through puncturing, shortening, or repetition. Advanced puncturing schemes preserve channel polarization and minimize performance loss. The Golden Decade survey identifies asymmetric puncturing and rate-compatible design as key enablers for 5G integration [10]. The 3GPP chose polar codes for uplink/downlink control channels in 5G-New radio, while LDPC codes serve data channels. Polar codes meet the 5G requirements of Reliability: up to 99.999%, Low latency: <1 ms. Flexibility: adaptable to short packets and variable rates [11]. In eMBB (Enhanced Mobile Broadband) and URLLC scenarios, polar codes provide the ideal compromise between latency and coding gain, while LDPC excels at very long block lengths [12]. Simulation studies confirm that polar codes outperform turbo codes under high-mobility and fading conditions, maintaining low BER and stable throughput even with severe Doppler effects.

Study demonstrates a polar-coded OFDM system tested in High-Speed Train (HST) channels [12]. The system mitigates Doppler and multipath effects using polar coding, achieving higher reliability and lower latency compared with LTE turbo codes. Key observations include: Polar encoding/decoding remains efficient for real-time systems. Performance improves with shorter code lengths suited for URLLC. Low-complexity SC/SCL decoders make hardware implementation feasible on FPGA and ASIC platforms.

4. Comparative Performance: Turbo vs. Polar Codes

The paper provides a detailed experimental comparison. Using Binary Phase Shift Keying (BPSK) modulation over AWGN channels, both coding schemes exhibit performance close to the Shannon limit [13]. Turbo Codes demonstrate superior BER performance for short and medium block lengths, especially under iterative decoding. Polar Codes outperform at large block lengths due to their asymptotic capacity-achieving property but lag at smaller lengths due to incomplete polarization. Turbo Codes have been integrated into 3G/4G LTE, while Polar and LDPC codes are standardized in 5G new radio—Polar for control channels and LDPC for data channels. These results emphasize that no single scheme universally dominates; rather, hybrid or concatenated schemes may combine the advantages of both. "Optimization of Iterative Decoding for Polar Product Codes" (Liu et al., 2024) introduces Weighted Factor (WF) optimization for iterative decoding of Polar Product Codes (PPCs). Product codes are constructed by encoding rows and columns separately using short component codes (e.g., Polar and Single Parity Check (SPC) codes).

The authors propose a Weighted Mean Square Error (WMSE) criterion to optimally adjust the decoding weights between row and column iterations. By fine-tuning these weights, they reduce error propagation during iterative decoding. The study compares Polar-Turbo polar codes and Polar-SPC-Turbo polar codes structures, demonstrating that optimized weighted factors yield significant performance gains compared to Monte Carlo-based tuning. This approach enhances decoding convergence and reduces complexity, offering a robust design for short-block-length communication scenarios. Two papers "Systematic Turbo-Polar, Turbo-LDPC-Polar and Turbo-LDPC Codes Based on Belief Propagation Decoding" (Umar et al., 2024) and its expanded version explore hybrid concatenated architectures that extend the Turbo principle to Polar and LDPC codes. The authors propose applying BP decoding over sparse factor graphs derived from Polar and LDPC codes. By pruning redundant nodes, the factor graph becomes sparse enough to support LDPC-style iterative decoding with reduced computational complexity [13].

Three hybrid schemes are proposed are Turbo-Polar Code – Two systematic Polar encoders concatenated in parallel. Turbo-LDPC-Polar – One Polar encoder and one LDPC encoder in parallel. Turbo-LDPC – Two LDPC encoders concatenated similarly. Simulation results reveal that Turbo-LDPC-Polar and Turbo-LDPC outperform standalone CA-SCL Polar codes (with list size 32) in both BLER and complexity for block lengths above 3072 bits. These designs achieve performance gains up to 0.5 dB at BLER = 10^{-4}, with significantly reduced decoding latency. Although Turbo-LDPC schemes are iterative and thus more complex than standard LDPC decoding, they remain computationally efficient compared to large-list SCL decoders [14]. The results validate the hybrid BP-based approach as a scalable path for future high-throughput 6G systems. "Polar Codes for Future Wireless Communications: Potential Applications and Design Guidelines" [15] addresses the main drawback of Polar codes—poor polarization in short block lengths by introducing Parity-Check-Concatenated structures. Polar Codes embed distributed parity bits within the Polar code structure, unlike Cyclic redundancy check-assisted schemes where parity is appended at the end [16]. This distributed mechanism improves error detection and correction by leveraging parity information throughout the codeword. Three major parity design methods are discussed:

I. Random Construction, where parity bits are randomly selected based on probability.
II. Heuristic Construction, based on observed error probabilities across bit-channel segments.
III. Minimal Construction, which minimizes the Cluster Pairwise Error Probability (CPEP) to reduce decoding path confusion.

The paper presents Parity-Check-Aided SCL (PCA-SCL) and Parity-Check-Aided Belief Propagation List (PCA-BPL) decoding. PCA-BPL, in particular, supports parallelism and achieves high throughput, making Polar codes attractive for hardware-efficient 5G control channels and potential 6G enhancements. Across the reviewed

works, a clear trend emerges—hybridization and iterative optimization are the dominant strategies for improving finite-length Polar code performance. Key insights include:

Hybrid Concatenation (Turbo-Polar, Turbo-LDPC-Polar, Polar) enhances both BER and convergence speed [15]. BP-based decoding transforms Polar codes into graph-based structures compatible with LDPC-like iterative techniques. Product codes introduce flexible design configurations for parallel processing and reduced latency. Structures effectively overcome polarization deficiencies in short codes.

Optimization techniques like weighted factors and pruning further improve performance while maintaining hardware feasibility [16].

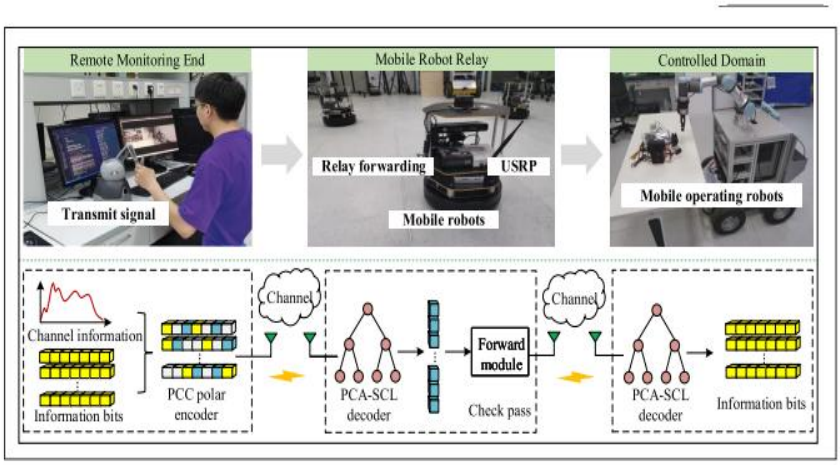

Figure 2: polar codes-based collaborative multi-robot communication system.[16]

Conclusion

This paper presents a comprehensive overview of Turbo codes, polar codes, and hybrid coding schemes relevant to modern wireless systems. Turbo codes achieve near-Shannon-limit performance through iterative decoding but face challenges of high latency and error floors. Polar codes, recognized as the first capacity-achieving codes and standardized in 5G New Radio (NR), offer low-complexity encoding yet exhibit limited performance at finite block lengths. To overcome these limitations, hybrid architectures such as Turbo-Polar and LDPC-Polar codes combine iterative and belief-propagation decoding techniques, achieving improved reliability, lower decoding complexity, and enhanced throughput. Comparative analyses show that Turbo codes are effective for large frames, Polar codes for short block lengths, and hybrid codes provide an optimal trade-off between performance and complexity. Overall, the integration of Turbo, Polar, and LDPC principles marks a key advancement in FEC for 5G and 6G systems, supporting ultra-reliable, low-latency, and energy-efficient communication.

Declaration of Conflicting Interests

The authors declare no potential conflicts of interest with respect to the research, authorship and publication of this article.

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